110', designed to attempt to minimize signal path discontinuities (e.g. variations in impedance). More particularly, the FIG. 5 embodiment has, for example, a core 310' and multiple build-up layers 320X', 340B', 350N' 340A', 350M' on the primary-side, and a lesser number of build-up layers, such as only one peripheral core conductive layer 320Y', on the substrate 110's secondary side (e.g., core bottom side). That is, the build-up layers 340C, 350P, 340D, 350Q that were present on the bottom side of the core 310 in the FIG. 4 arrangement have been reduced, or eliminated. Practice of embodiments of the present invention is not limited to this specific arrangement, and instead, other example embodiments may be where the substrate mounting-side of the arrangement has one-quarter, one-third or even one-half a number of conductive layers as opposed to a number of the primary-side of the package.

The paragraph beginning on page ~~13~~ 11, line ~~6~~ 5 is amended as follows: SM 11/12/07

In concluding, in such FIG. 5 example embodiment, there may occur a lesser variation between a mounting-component-side signal entering the bottom of the substrate 110, and the primary-side signal leaving the substrate to enter the die 120. While the example embodiment was described as reducing any [[an]] impedance and physical joint discontinuities at an input/output of a secondary side of the substrate 110', practice of the present invention can just as easily be applied to reduce discontinuities at an input/output of a primary (die) side, or even within internal layers of the substrate. For example, if a localized impedance discontinuity is determined to exist along an internal signal path as a result of parasitic capacitance between ones of the internal layers (e.g., neighboring vertical vias), modifications (e.g., increased separation distance; changing of a material there-between to one having a differing permittivity) may be used to reduce the localized impedance discontinuity to within a predetermined acceptable range.